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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/994,395	11/26/2001	Sergey D. Lopatin	039153-0457 (G1162)	7882

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EXAMINER	
MAGEE, THOMAS J	
ART UNIT	**PAPER NUMBER**
2811	

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Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 07-01)

Office Action Summary	**Application No.** 09/994,395	**Applicant(s)** LOPATIN ET AL.	
	Examiner Thomas J. Magee	**Art Unit** 2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 July 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 4 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections – 35 U.S.C. 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 4 and 5 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Applicant is referring to "resistivity" rather than "resistance", as interpreted from the units recited. Examiner assumes that this may have been a simple typographical error.

3. Claim 22 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Applicant refers to "staffed grain boundaries." Examiner again assumes that this is a typographical error and Applicant meant to recite "stuffed grain boundaries." Applicant is advised that the error is found throughout the Specification and should be corrected.

Claim Rejections – 35 U.S.C. 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office Action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1 - 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Edelstein et al. (US 6,399,496 B1) in view of Andricacos et al. (US 6,090,710), Tsuji et al. (5,004, 520), and Bogel et al. (US 2002/0039542 A1).

6. Regarding Claim 1, Edelstein et al. disclose a method for fabricating an interconnection structure used on a device in an integrated circuit wherein a barrier layer (72) (Figure 2) (Col.10, lines 59 – 62) is formed along the lateral sidewalls and bottom of a via aperture, where the via aperture is configured to receive a via material that connects a first and second conductive layer. Edlestein et al. further disclose (Col. 6, lines 26 – 52) that the via material comprises copper and a copper alloy with at least one element from the group, Sn, In, Zr, Ti, C, O, N, Cl or S, to improve resistance to electromigration, or at least one element from the group, B, O, N, P, Fe, Ru, Os, Co, Rh, Ir, Ni, Pd, Pt, Ag, Zn, or Cd, to improve surface properties, or at least one element from the group, Ca, Sr, Cr, Be, Mg and others to improve adhesion. In like fashion, Andricacos et al. disclose (Col. 3, lines 38 – 65) a method for forming copper interconnects within devices on chips wherein at least one alloying element is selected from the group, C, In, or Sn, for improved electromigration resistance and low resistivity. Andricacos et al. disclose (Col.8, lines 43 – 54) that a ternary alloy (more than one added element to copper) can be used to achieve the same results. Although Edelstein et al. do not explicitly disclose a ternary alloy, more than one element could be included in the copper alloy and it would be

obvious to include additional elements (Col. 8, lines 49 – 52) based on the application of Bogel et al. (page 1, paragraphs [0003] and [0005]) where bulk alloy (multi-element) materials are disclosed for use as electrical connectors with low conductivity, and Tsuji et al. (Col. 10, 67 – 68, Col. 11, lines 1 – 3) wherein copper alloys containing one or more elements from the group, In, Sn, and Ag, are disclosed for use in foils for mounting components and IC's. It would then be obvious to set up a DoE to determine (or optimize) the best alloying elements for robust Cu conductive regions. Further, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine Andricacos et al., Tsuji et al., and Bogel et al. with Edelstein et al. to produce a ternary Cu alloy that would provide lower resistivity and increased electromigration resistance.

7. Regarding Claims 2 and 3, Edelstein et al. do not explicitly disclose that the resistance is lowered with copper alloys, but Andricacos et al. disclose (Col. 8, lines 43 – 54) that low resistivity (resistance) is obtained with ternary copper alloys containing In, C, or Sn. Hence, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine Anricacos et al., Tsuji et al., and Bogel et al. with Edelstein et al. to obtain low resistance Cu alloy conductive regions.

8. Claims 4 and 5, in so far as being in compliance with 35 U.S.C. 112, second paragraph, are rejected under 35 U.S.C. 103(a) as being unpatentable over Edelstein et al. in view of Andricacos et al., Tsuji et al., and Bogel et al.

Edelstein et al. disclose that the Sn is contained within the copper alloy at a level of

0.25 to 1.5 atomic percent (Col. 10, lines 1 – 3) but do not disclose a resistivity value. Andricacos et al. disclose (Col. 8, Table 1) that the resistivity of copper alloys containing one percent or less of Sn and other alloying elements is in the range, 1.9 to 3.1 micro-ohm-cm, which is in the range recited in the instant application. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to use the resistivity data of Andricacos et al. in Edelstein et al. to produce Cu multi-element alloys of varying resistivity and to combine Andricacos et al., Tsuji et al., and Bogel et al. with Edelstein et al.

9. Claims 6 – 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Edelstein et al. in view of Andricacos et al., Tsuji et al., and Bogel et al., as applied to Claims 1 – 3, and further in view of Cunningham ("Improving Copper Interconnects: A search for Useful Dopants," Semiconductor International, April, 2000, pp. 1 – 8), and Harper et al. (US 5,243,222).

Edelstein et al. do not disclose the effect of alloying elements on grain size, but do disclose the use of alloying elements Ca and Cr within the copper seed layers. Harper et al. disclose that alloying element additions of less than one atomic percent Cr are used in producing Cu alloy interconnect structures (plugs) that exhibit high current density tolerances (Col. 6, lines 2 – 14). Cunningham discloses that in electrochemically deposited (plated) alloyed layers subsequent to annealing, the "doped" (alloyed) material exhibits growth of grains to a size of 1 - 5um (page 3, 1st paragraph) with columnar structure. It would have then been obvious to combine Cunningham and

Harper et al. with Edelstein et al.,Andricacos et al.,Tsuji et al., and Bogel et al. to obtain stable Cu alloy regions that exhibit large grains from alloy element additions, thereby increasing current carrying capacity and resistance to electromigration.

10. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Eddelstein et al. in view of Cunningham.

Edelstein et al. disclose a method of using a ternary copper alloy (Col. 8, lines 49 – 52) to obtain interconnect or via structures in which a first conductive layer (46) (Figure 2) is provided over an integrated circuit substrate, followed by the formation of a conformal layer (72) at the bottom and sides of a via aperture (60) to form a barrier layer separating the via from the first conductive layer. Further, Edelstein et al. disclose that the via aperture is filled with copper alloy to form a ternary via and a second conductive layer (56) formed over the via, electrically connecting first and second conductive layers. Edelstein et al. do not explicitly disclose that the addition of select alloying elements will yield low resistance or increases in grain size within the copper vias. However, Cunningham discloses (page 5, Figure 4) that a number of elements within a copper alloy produce low resistivity (resistance). In addition, Cunningham discloses that in electrochemically deposited (plated) alloyed layers subsequent to annealing, the "doped" (alloyed) material exhibits growth of grains to a size of 1 - 5um (page 3, 1st paragraph) with columnar structure. It would have then been obvious at the time of the invention to one of ordinary skill in the art to combine Cunningham with Edelstein et al.

to obtain ternary alloy vias of low resistance and large grain size to improve reliability and improve resistance to electromigration.

11. Claims 11 – 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Edelstein et al. in view of Cuinningham, as applied to Claim 10, and further in view of Andricacos et al.

Edelstein et al. do not explicitly disclose that the resistance is lowered with copper alloys, but do disclose that Sn is contained within the copper alloy at a level of 0.25 to 1.5 atomic percent (Col. 10, lines 1 – 3). Andricacos et al. disclose (Col. 8, lines 43 – 54) that low resistivity (resistance) is obtained with ternary copper alloys containing In, C, or Sn. Hence, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine Cunningham and Andricacos et al. with Edelstein et al. to obtain low resistance (resistivity) copper alloys for vias.

12. Claims 14 – 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Edelstein et al. in view of Cunningham, as applied to Claim 10, and further in view of Harper et al.

Edelstein et al. do not disclose the effect of alloying elements on grain size, but do disclose the use of alloying elements Ca and Cr within the copper seed layers. Harper et al. disclose that alloying element additions of less than one atomic percent Cr are used in producing Cu alloy interconnect structures (plugs) that exhibit high current density tolerances (Col. 6, lines 2 – 14). Cunningham discloses that in electrochemically

deposited (plated) alloyed layers subsequent to annealing, the "doped" (alloyed) material exhibits growth of grains to a size of 1 - 5um (page 3, 1st paragraph) with columnar structure. It would have then been obvious to combine Cunningham and Harper et al. with Edelstein et al et al., to obtain stable Cu alloy regions that exhibit large grains from alloy element additions, thereby increasing current carrying capacity and resistance to electromigration.

13. Claims 17 – 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Edelstein et al.

14. Regarding Claim 17, Edelstein et al. disclose a method of forming a via in an integrated circuit wherein a first conductive layer (46) (Figure 2) is formed, followed by deposition of an etch stop layer (101) over the first conductive layer and an insulating layer (54) over the etch stop layer, whereupon an etch is applied and an aperture formed in the insulating layer and etch stop layer. Edelstein et al. further disclose that a barrier material (72) is deposited on the bottom and sides of the aperture, followed by a ternary (Col. 8, lines 49 – 52) Cu fill (seed layer, 76, and via material, 60.) (Figure 2) and formation of a second conducting line (56), where the via electrically connects the first and second conductive layers.

15. Regarding Claim 18, Edelstein et al. disclose that a ternary alloy (Col. 8, lines 49 – 52) can be formed using Cu, Sn (Col. 8, lines 31 – 34) and Cr (Col. 8, lines 35 – 41).

16. Regarding Claim 19, Edelstein et al. disclose that a ternary alloy (Col. 8, lines 49 – 52) can be formed using Cu, Zn (Col. 8, lines 42 – 45) and Cr (Col. 8, lines 35 – 41).

17.Regarding Claim 20, Edelstein et al. disclose that a ternary alloys (Col. 8, lines 49 – 52) can be formed comprising the following: CuAgCr (Col 8, lines 35 – 45), CuSnCa (Col. 8, lines 31 – 41), and CuAgCa (Col. 8, lines 35 – 45).

18. Claims 21 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Edelstein et al., as applied to Claims 17 – 20 above, and further in view of Cunningham. Edelstein et al. do not disclose the effect of alloying elements on grain size. Cunningham discloses that in electrochemically deposited (plated) alloyed layers subsequent to annealing, the "doped" (alloyed) material exhibits growth of grains to a size of 1 - 5um (page 3, 1st paragraph) with columnar structure.

19. Claim 22, in so far as being in compliance with 35 U.S.C. 112, is rejected under 35 U.S.C. 103(a) as being unpatentable over Edelstein et al., as applied to Claims 17 - 20 above, and further in view of Cunningham.
Edelstein et al. do not disclose the stuffing of grain boundaries. Cunningham discloses that within the copper alloy, precipitation of elements and compound formation occurs at the grain boundaries (page 5, 1st paragraph). It would have then been obvious to combine Cunningham with Edelstein et al. to obtain copper alloys with large grains and Localized precipitation at grain boundaries to increase resistance to electromigration.

Conclusions

Any inquiry concerning this communication or earlier communications from the Examiner should be directed to **Thomas Magee**, whose telephone number is **(703) 305 5396.** The Examiner can normally be reached on Monday through Friday from 8:30AM to 5:00PM (EST). If attempts to reach the Examiner by telephone are unsuccessful, the examiner's supervisor, **Tom Thomas**, can be reached on **(703) 308-2772.**. The fax number for the organization where this application or proceeding is assigned is **(703) 308-7722.**

Thomas Magee
February 2, 2003

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